Digitaali- ja analogiaelektroniikan rajapinta

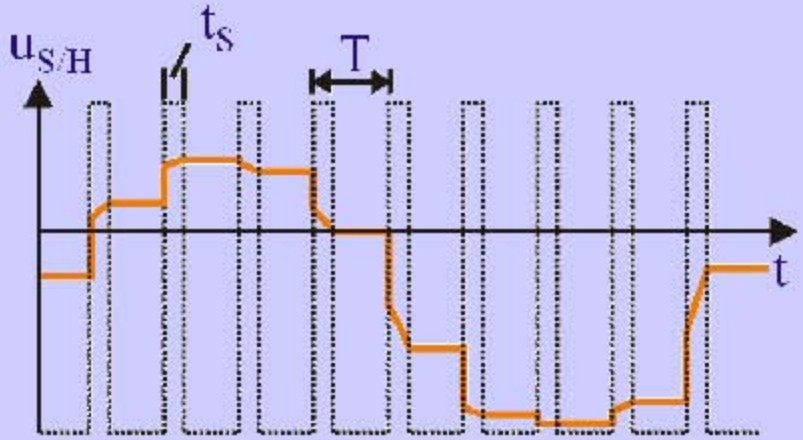
Datamuuntimet

Määritelmiä

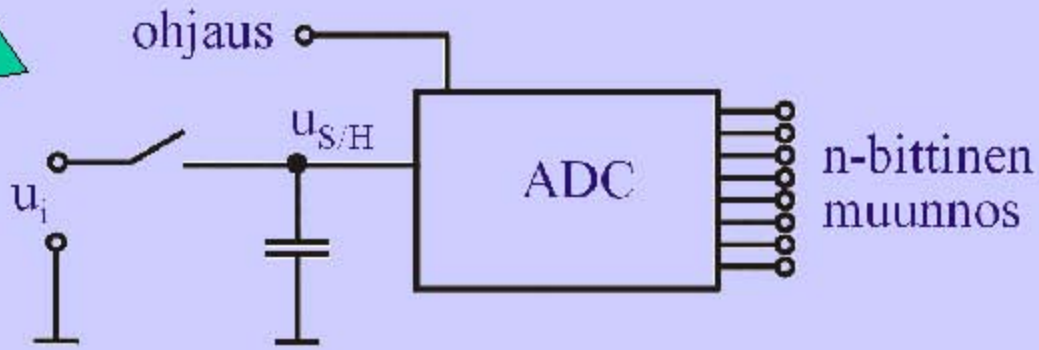
AD-muunnnos

u_i analogiasignaali

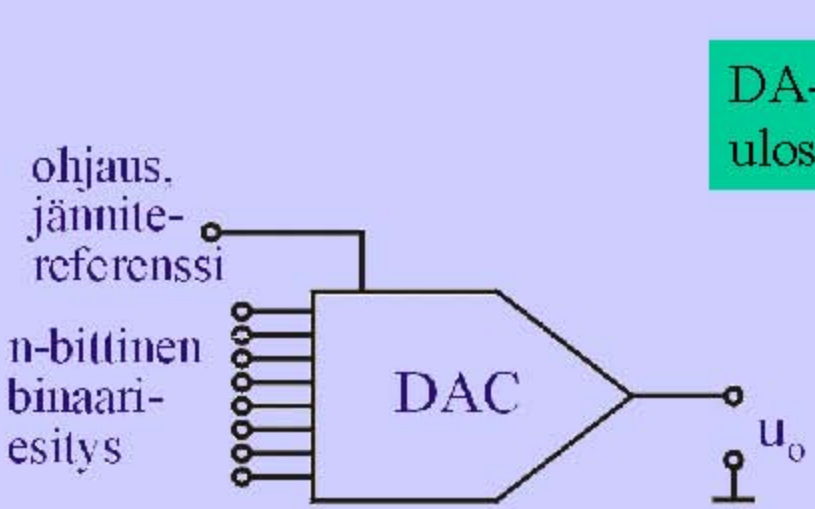
digitaalisignaali

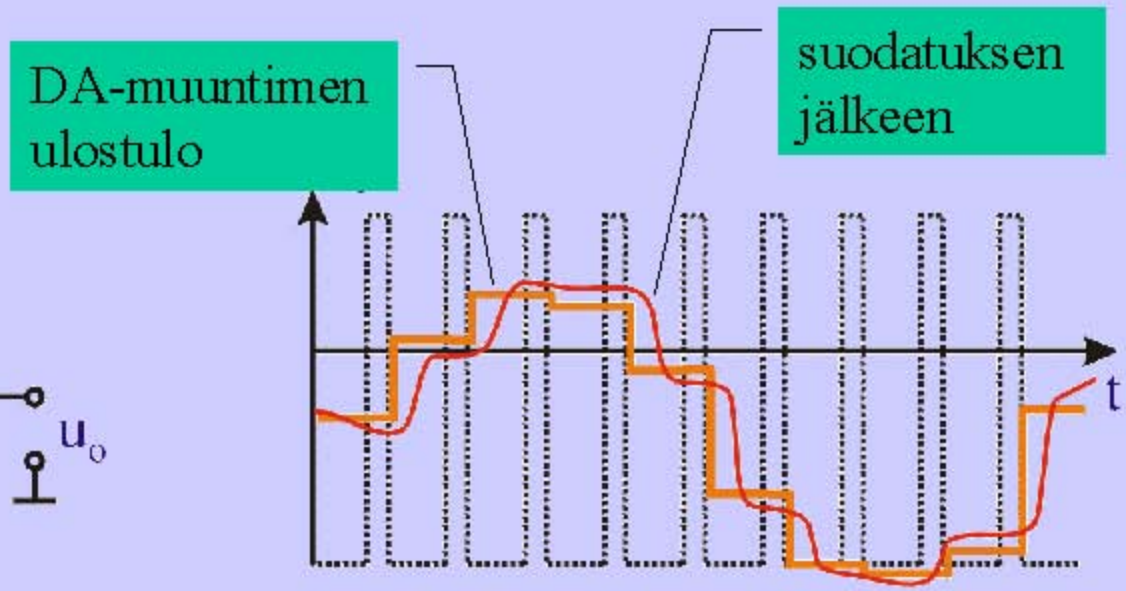


näytteistys-piiri



DA-muunnnos

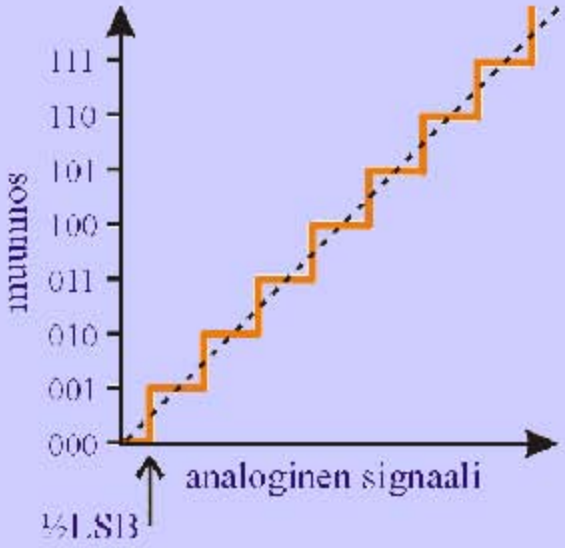

ohjaus,
jännite-
referenssi
n-bittinen
binaari-
esitys
DAC
u_o


DA-muuntimen
ulostulo
suodatuksen
jälkeen
t

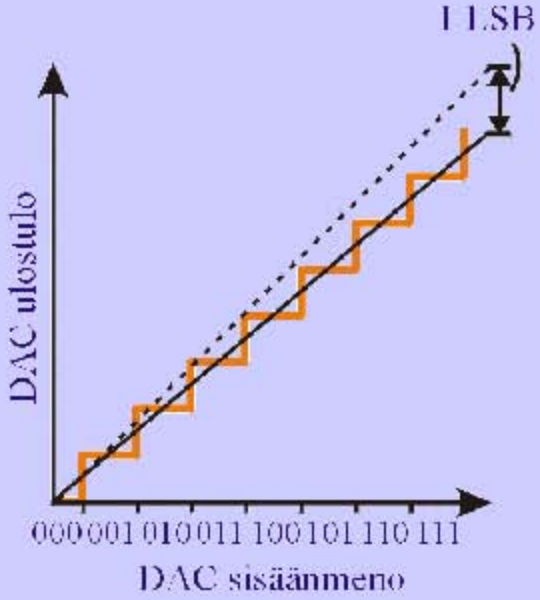
Datamuuntimien tärkeimmät parametrit

Parametri	**Merkitys**	**Lukuarvo**
Erotuskyky, *resolution*	määrää pienimmän sisäänmenosignaalin (tai ulostulosignaalin) muutoksen, jonka muunnin pystyy havaitsemaan (ADC) (tai toteuttamaan (DAC))	4 - 24 bittiä
Näytteenottotaajuus, *sampling rate*	Muuntimen sekunnissa suorittamien muunnosten määrä	3 Hz - 1 GHz
Muunnosaika, *conversion time*	Yhteen muunnokseen kuluva aika	1 ns - 1 s
Näytteenottoaika, *acquisition time*	Näytteenottopiirin näytteen ottamiseen vaatima aika	0,5 ns - 1 s

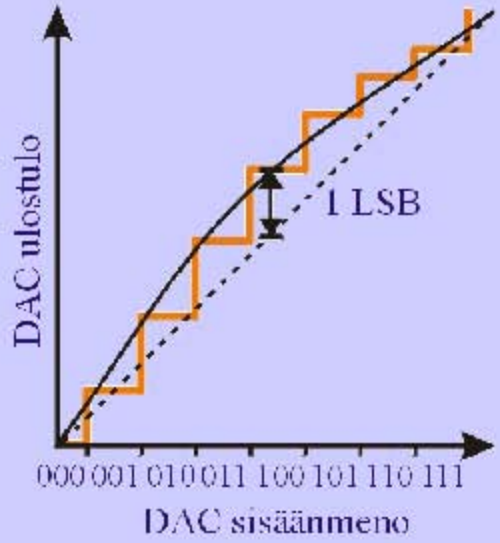
Datamuunnokset virhetyyppejä



kvantisointivirhe

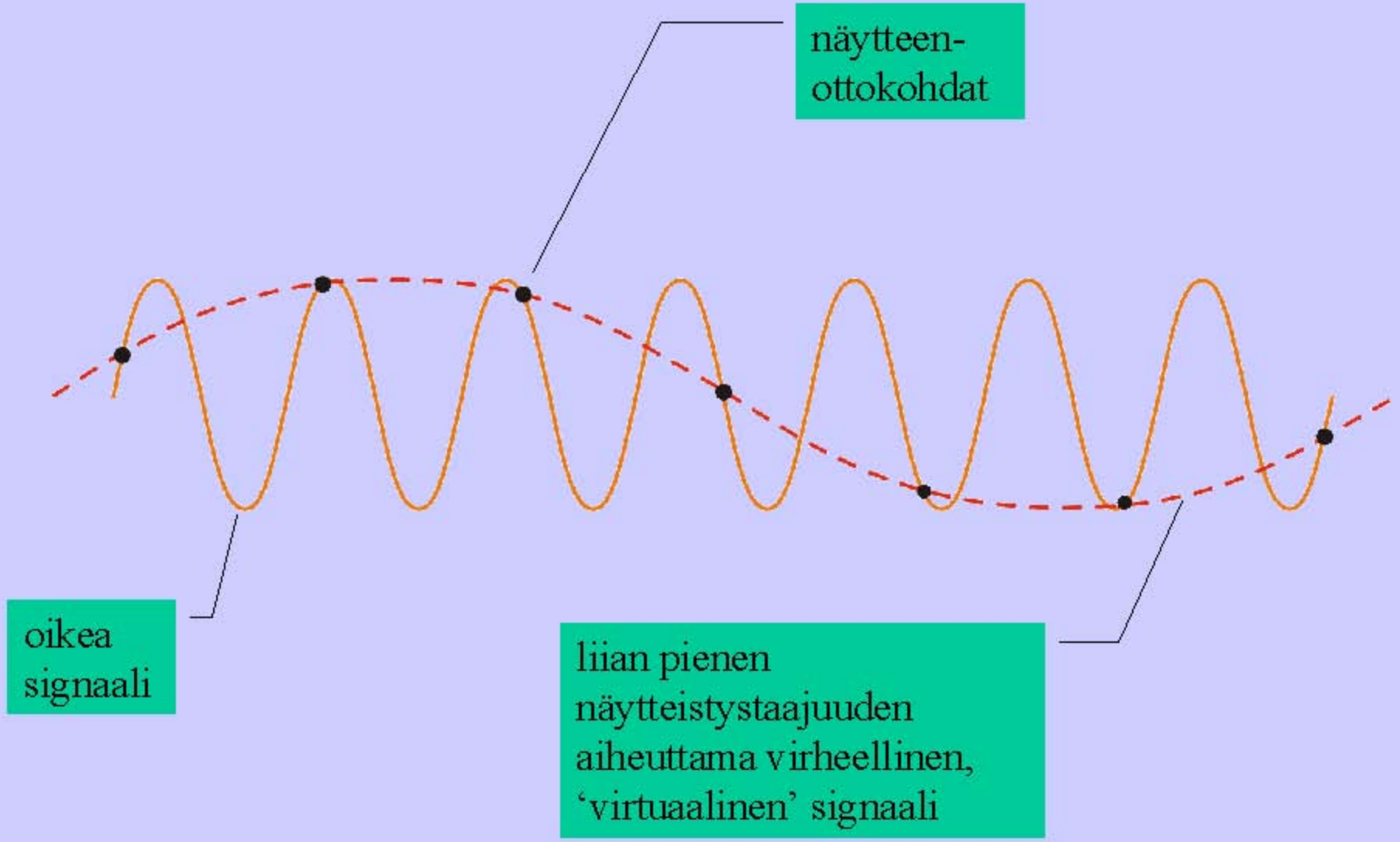


vahvistusvirhe

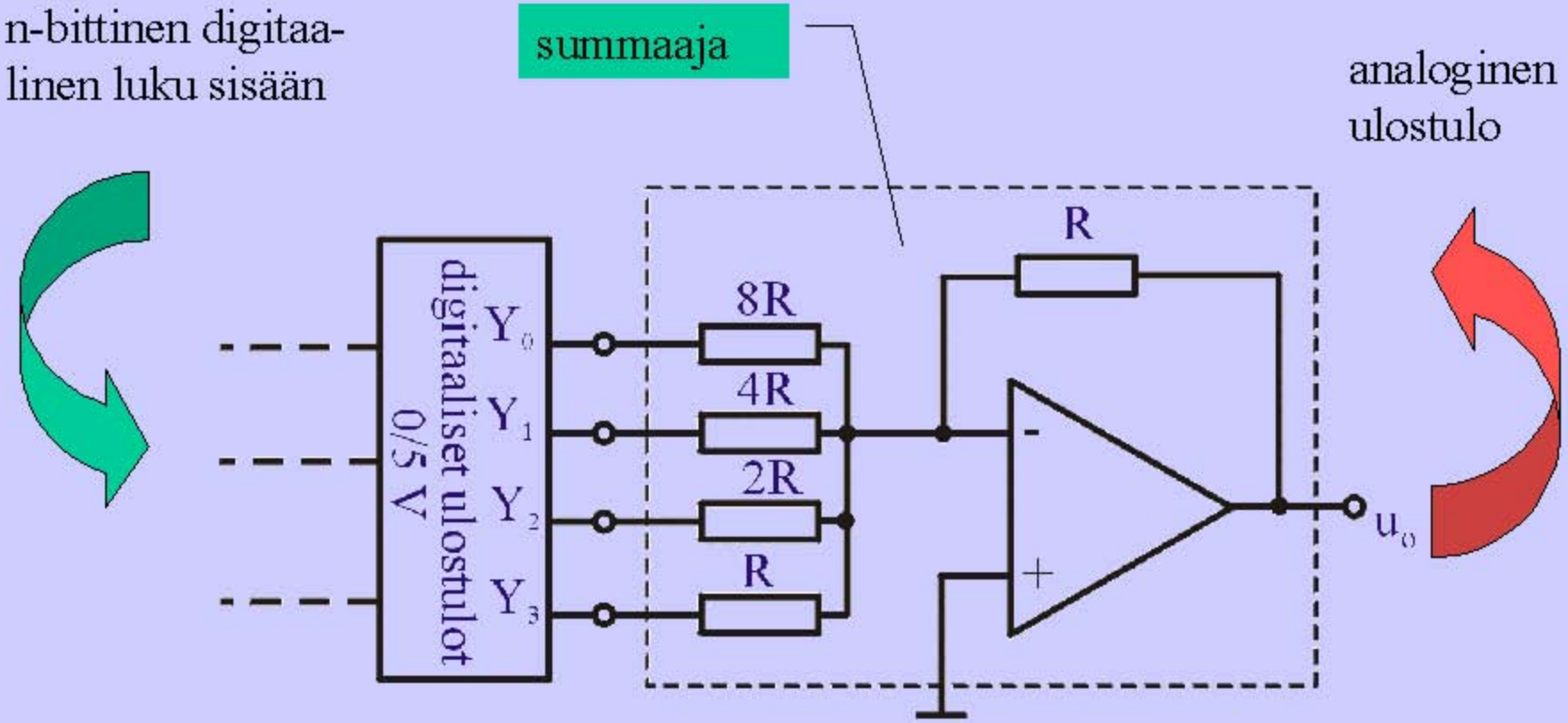


epälineaarisuus

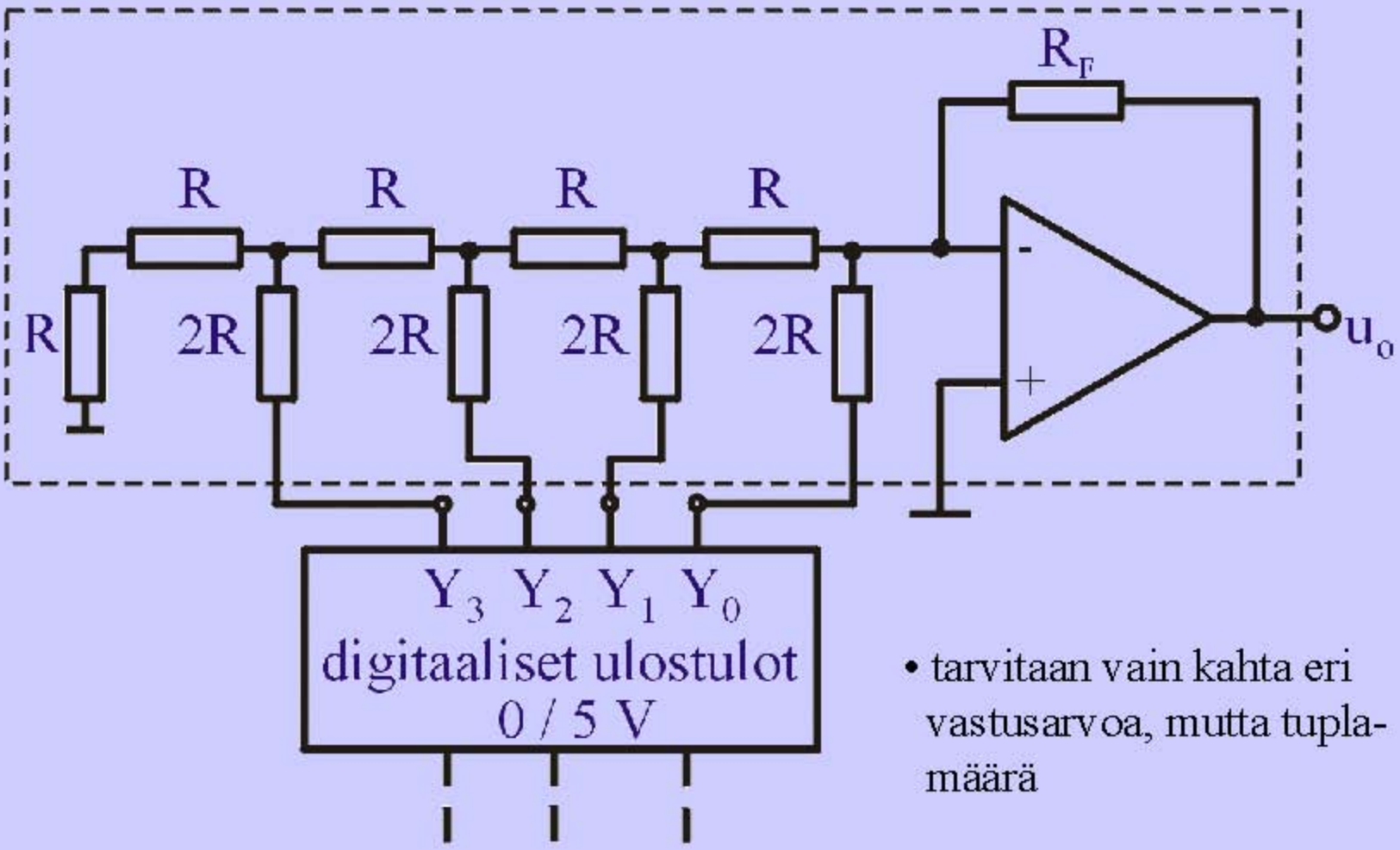
Aliasing


näytteen-
ottokohdat
oikea
signaali
liian pienen
näytteistystaajuuden
aiheuttama virheellinen,
'virtuaalinen' signaali

DA-muuntimien rakenteita



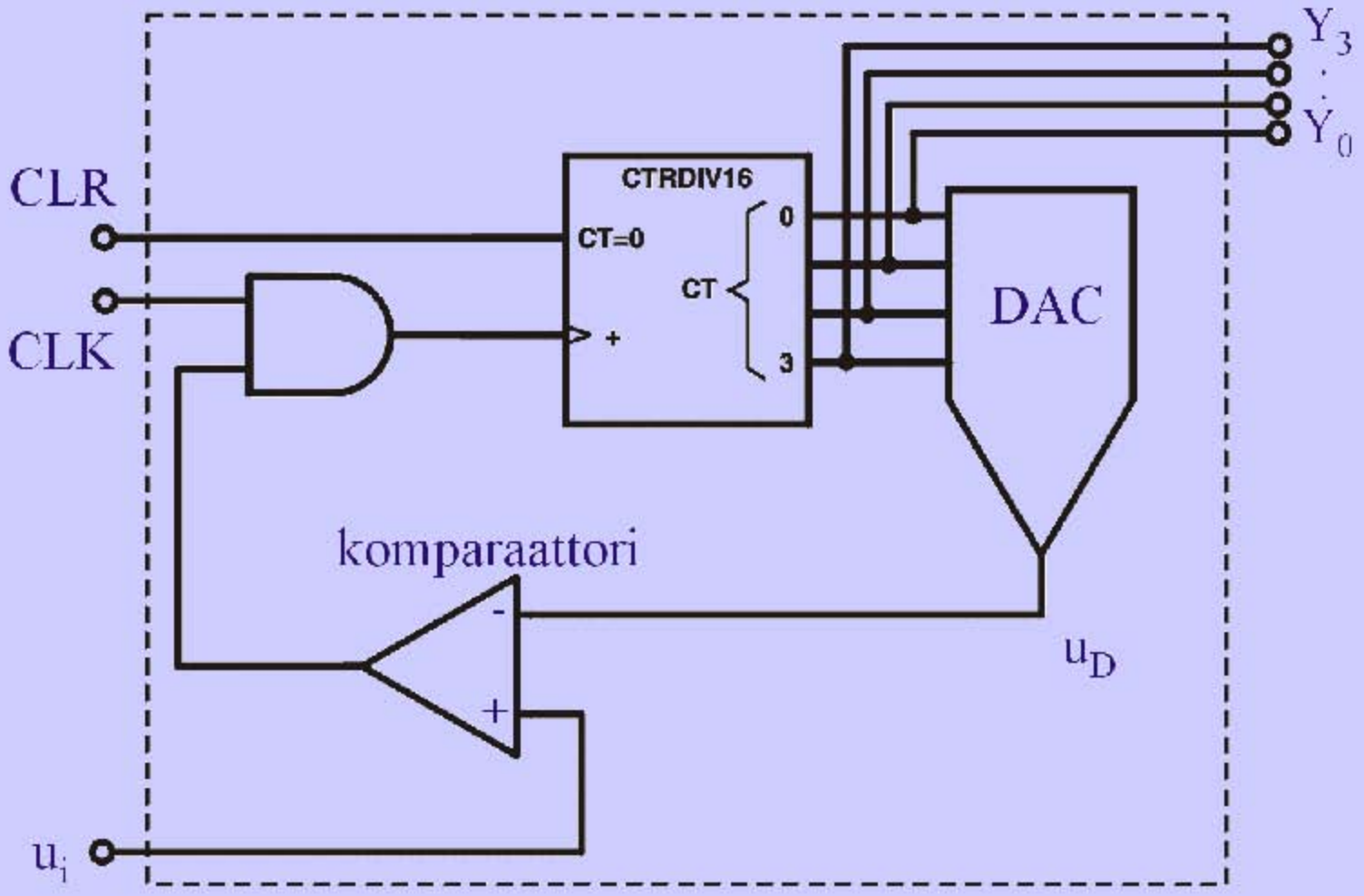
R-2R *ladder*, tikapuurakenne



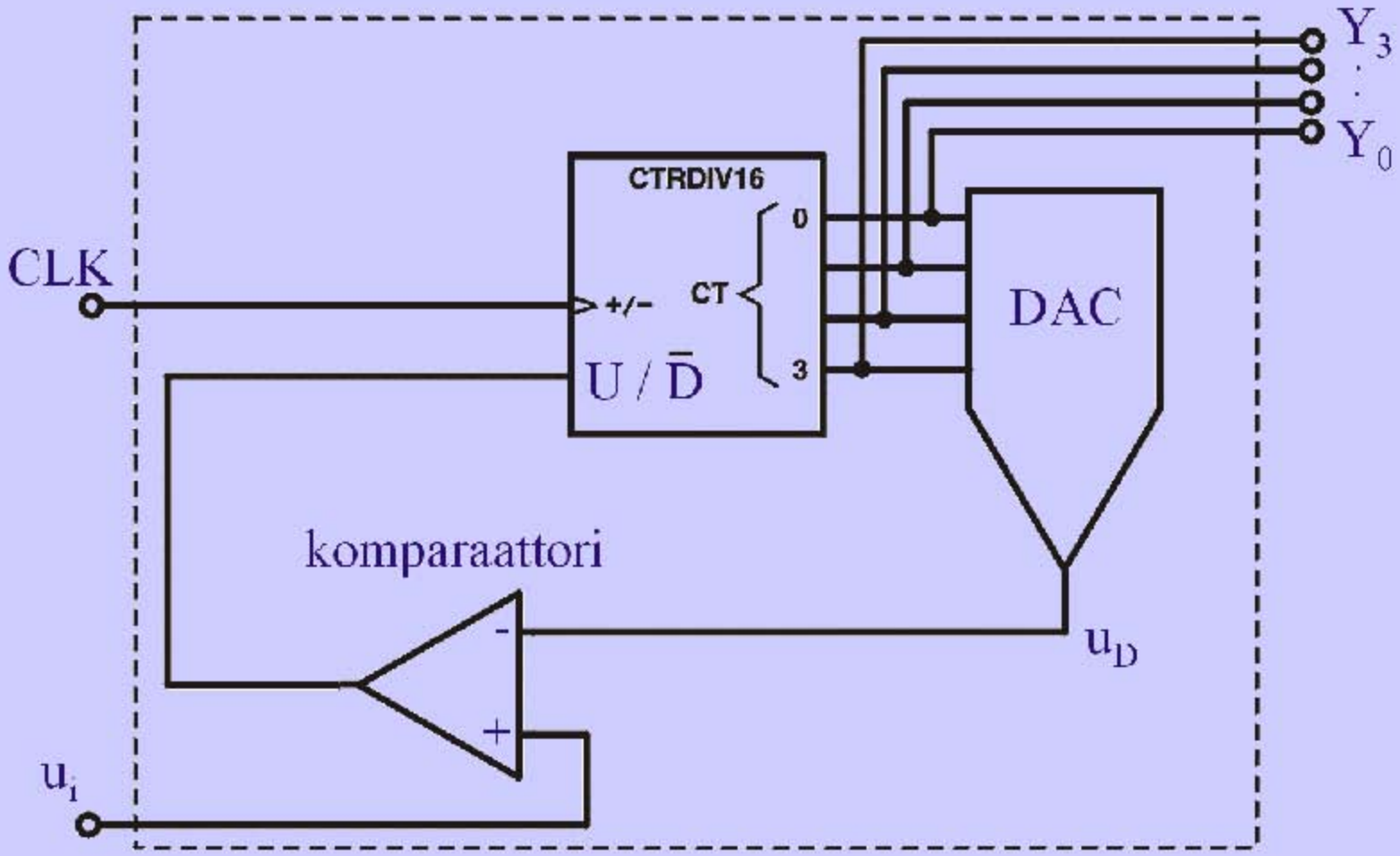
- tarvitaan vain kahta eri vastusarvoa, mutta tupla-määrä

AD-muuntimien rakenteita

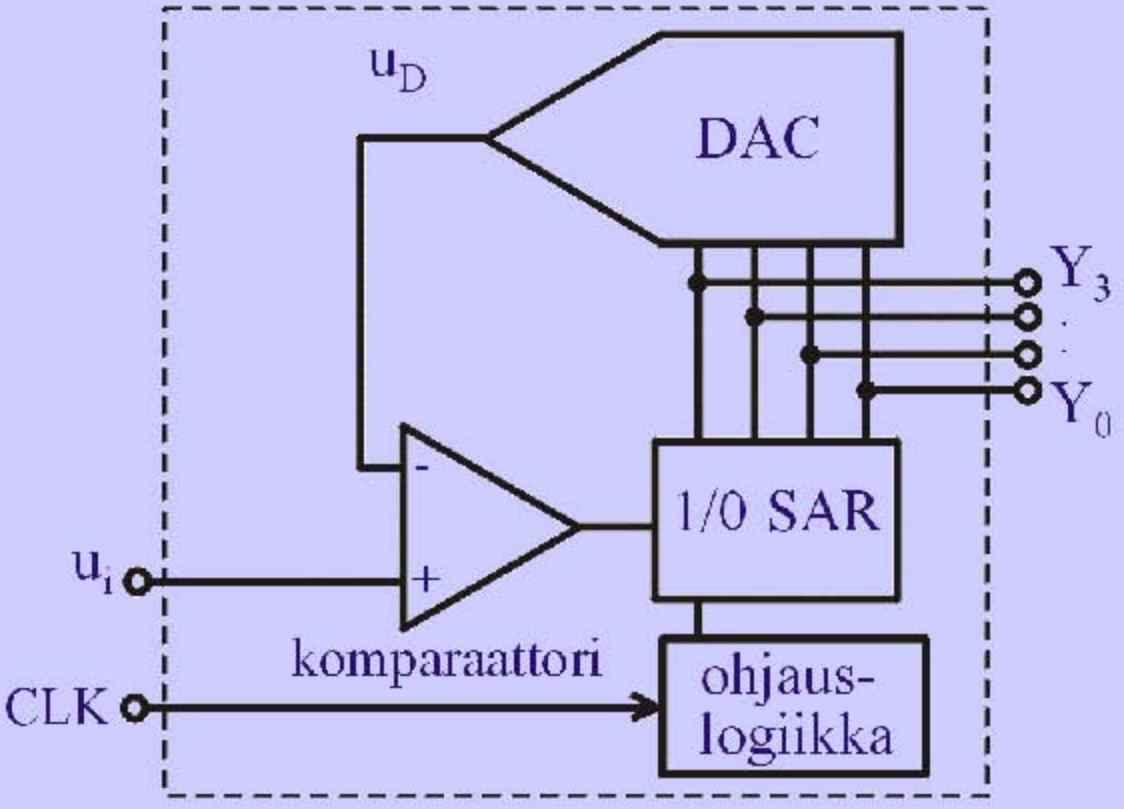
laskurityyppi

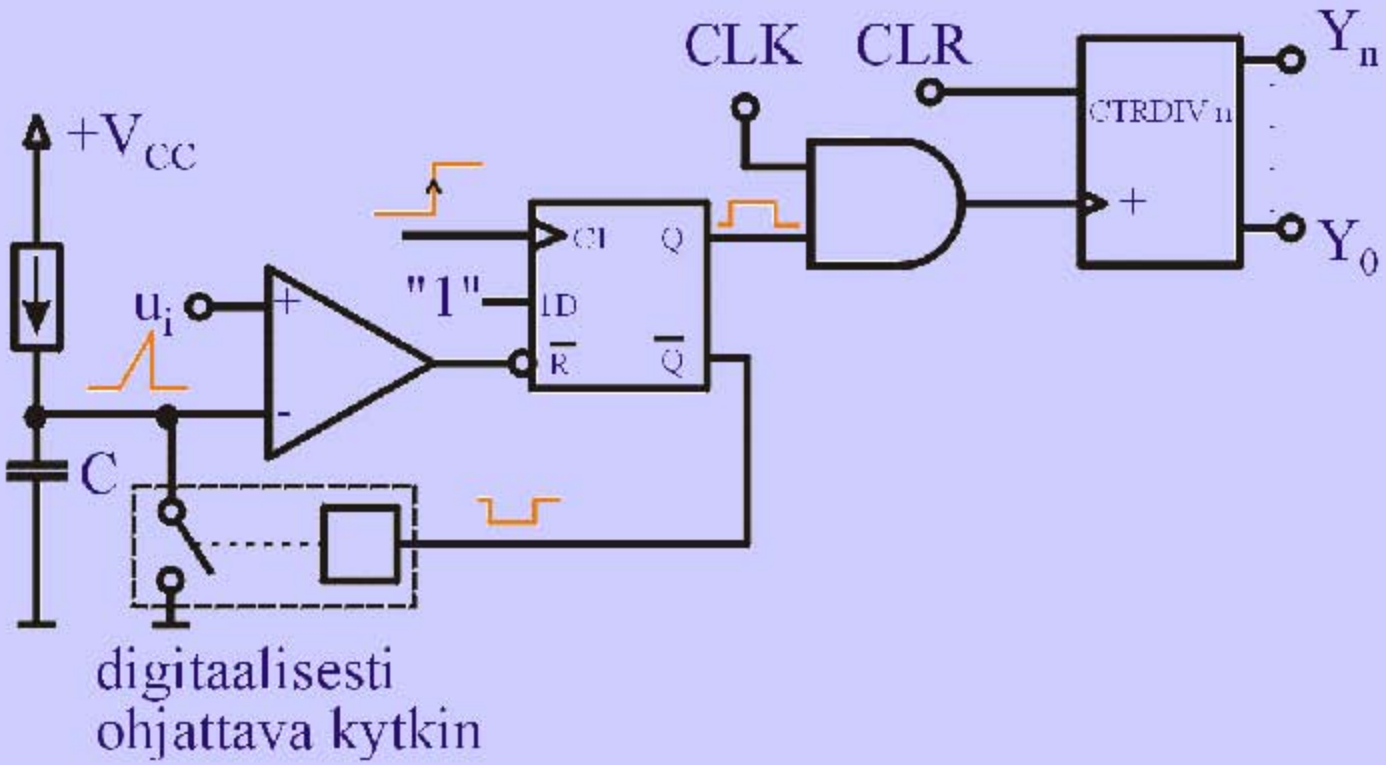


Tracking, seuraava

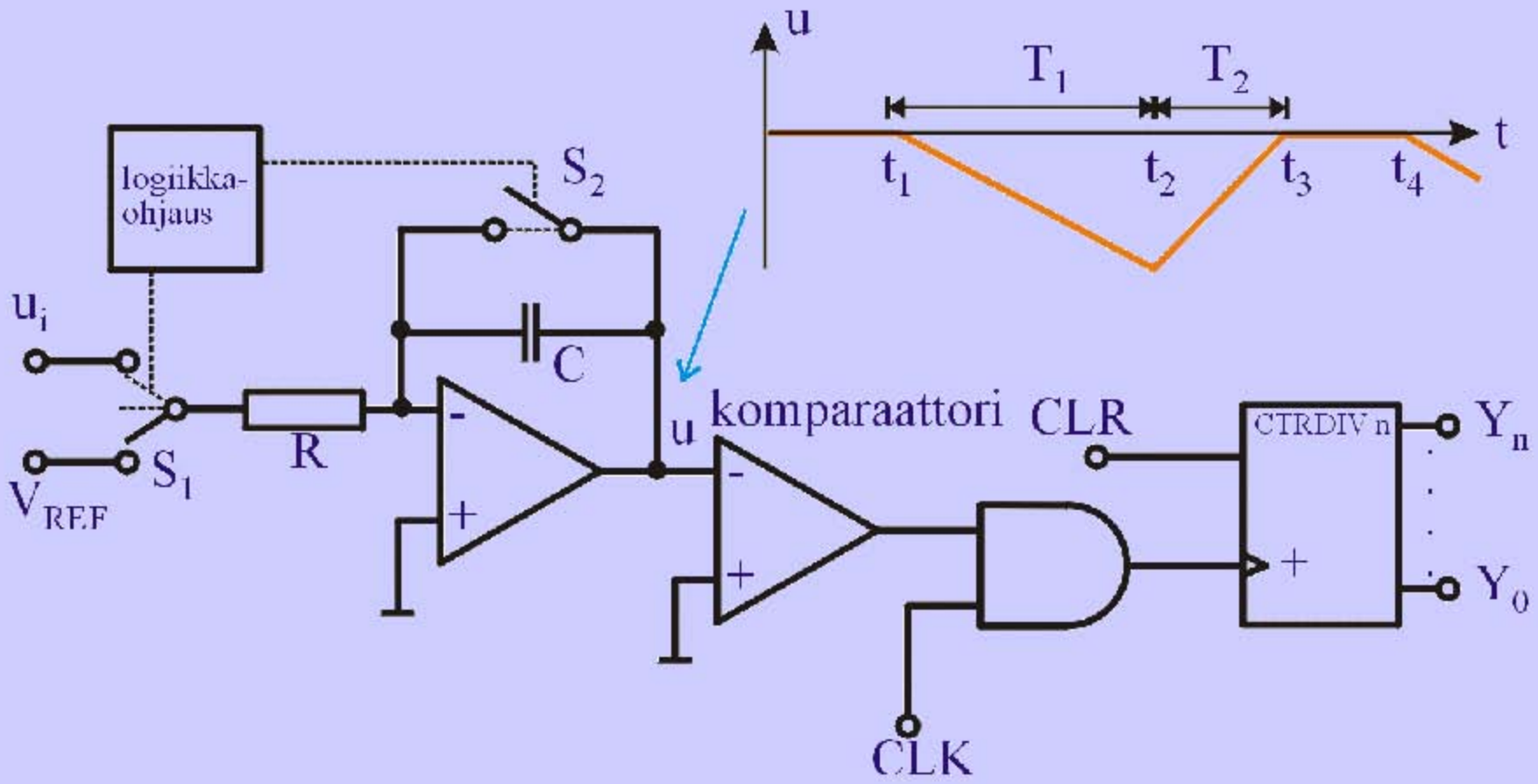


SA (successive approximation)

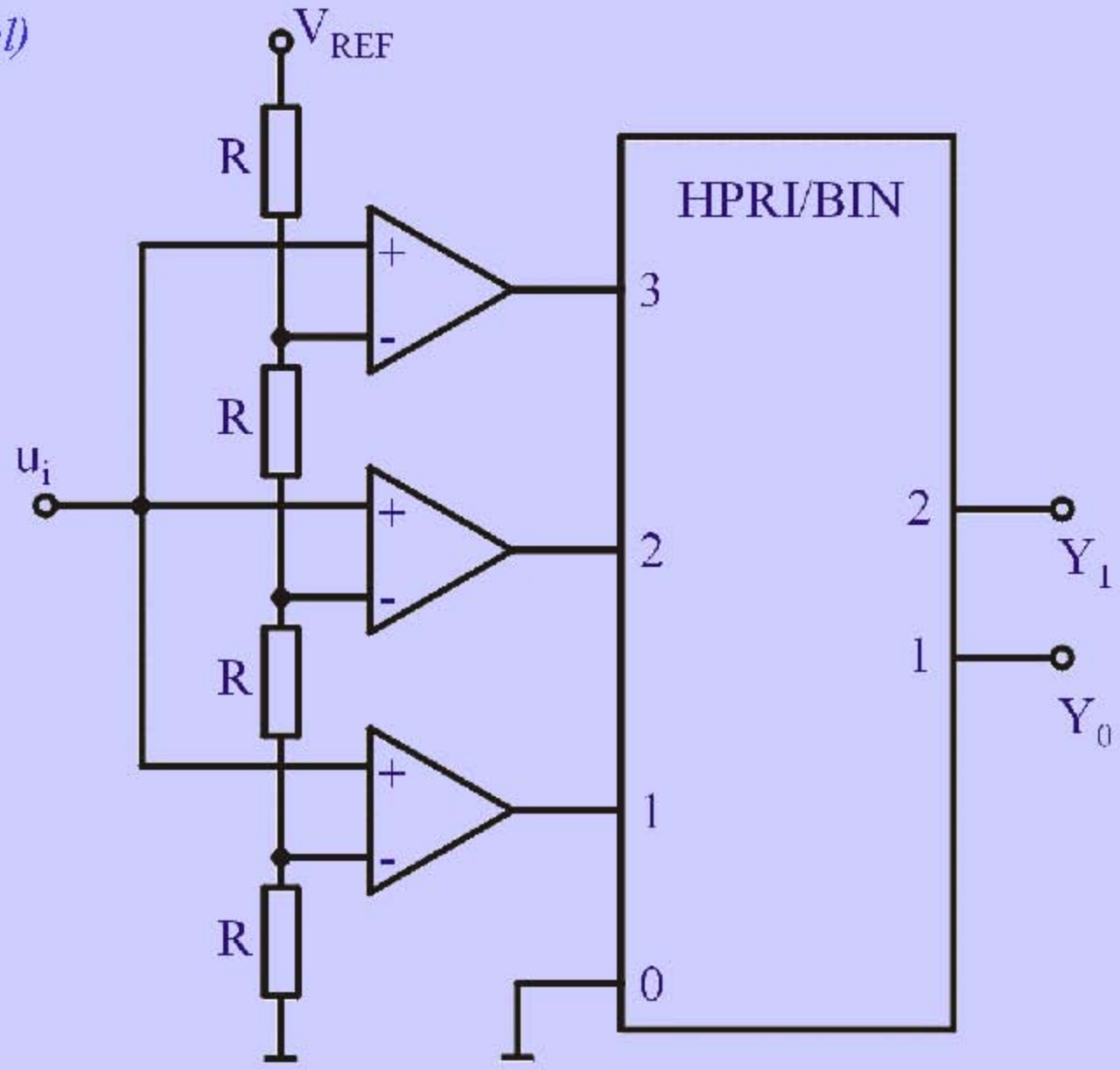



CLK
CLR
Y_n
CTRDIV n
+
Y_0
$+V_{CC}$
u_i
"1"
Cl
Q
1D
R
Q
C
digitaalisesti
ohjattava kytkin

Dual-slope (ratiometric)

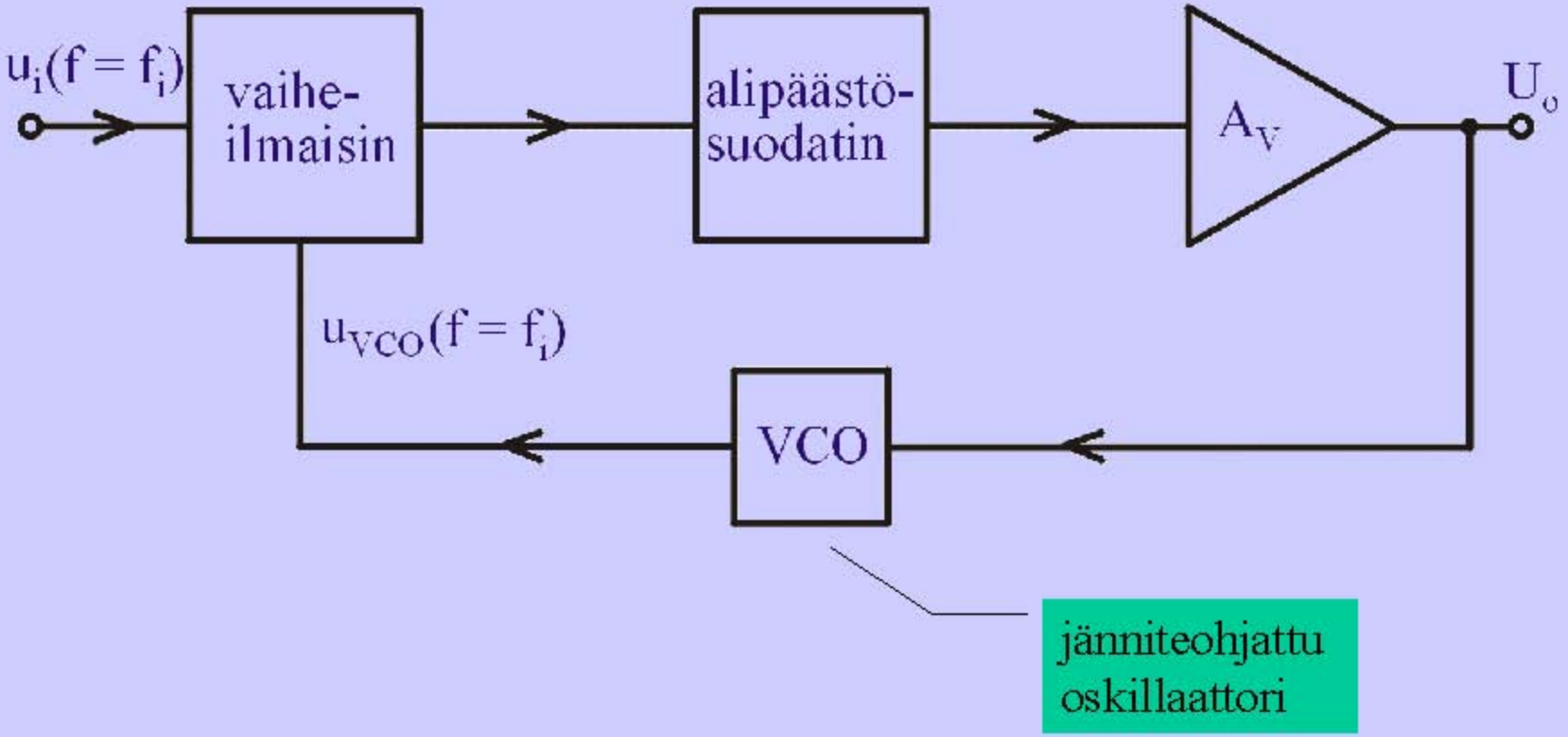


Flash (parallel)



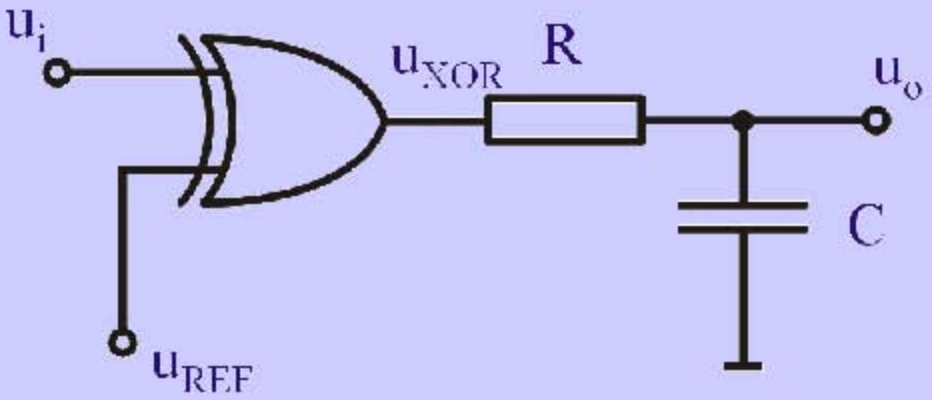
PLL- vaihelukkopiirit

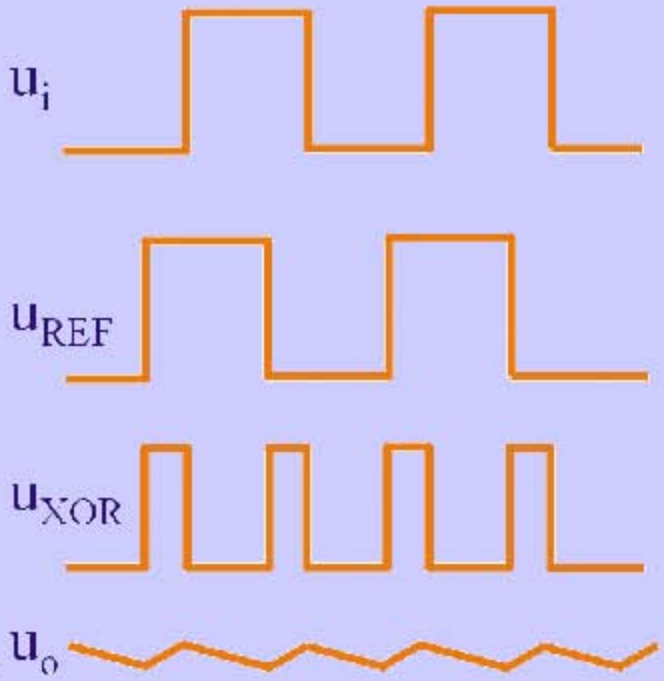
Periaate



Vaiheilmaisin

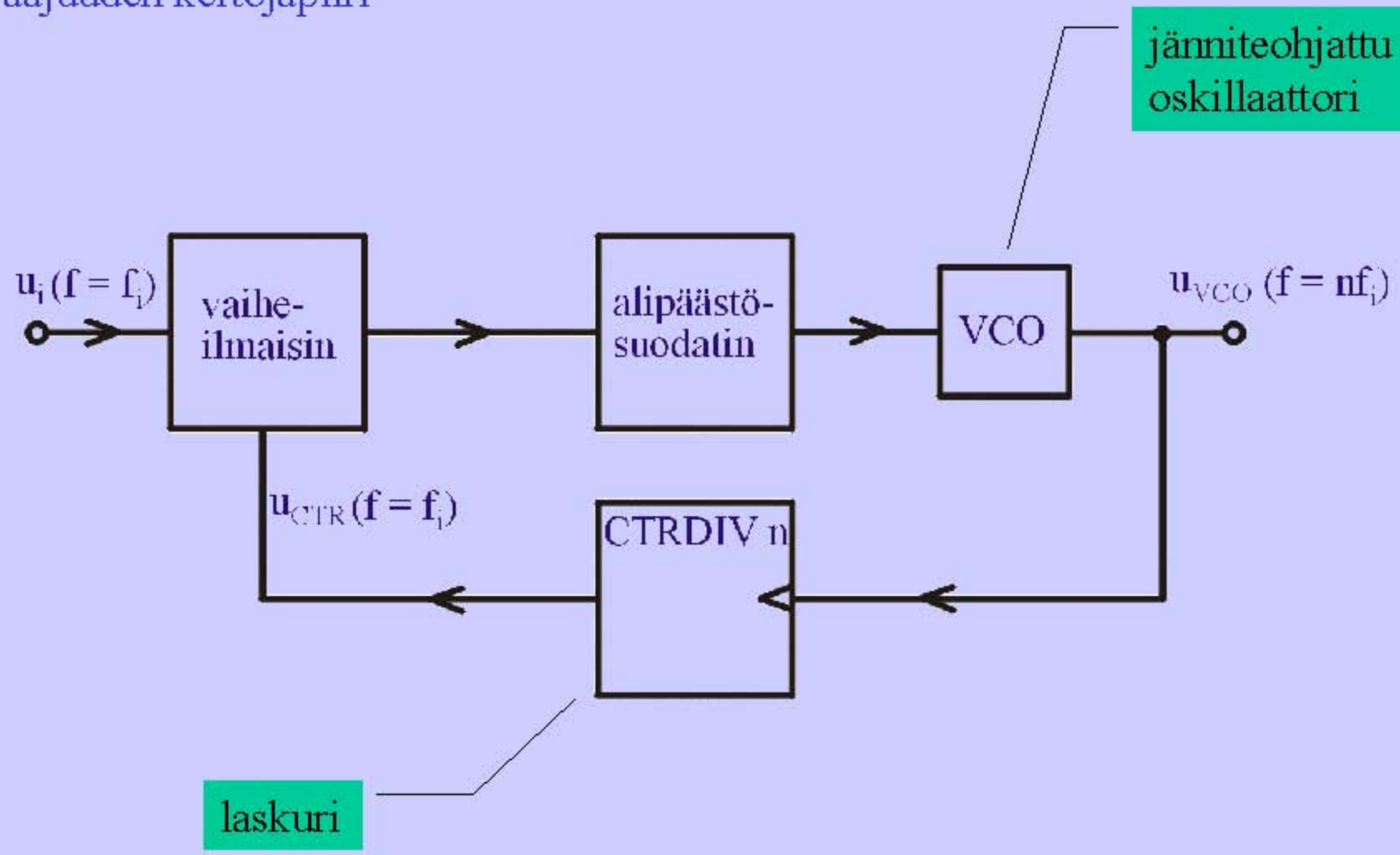
yksinkertainen ratkaisu



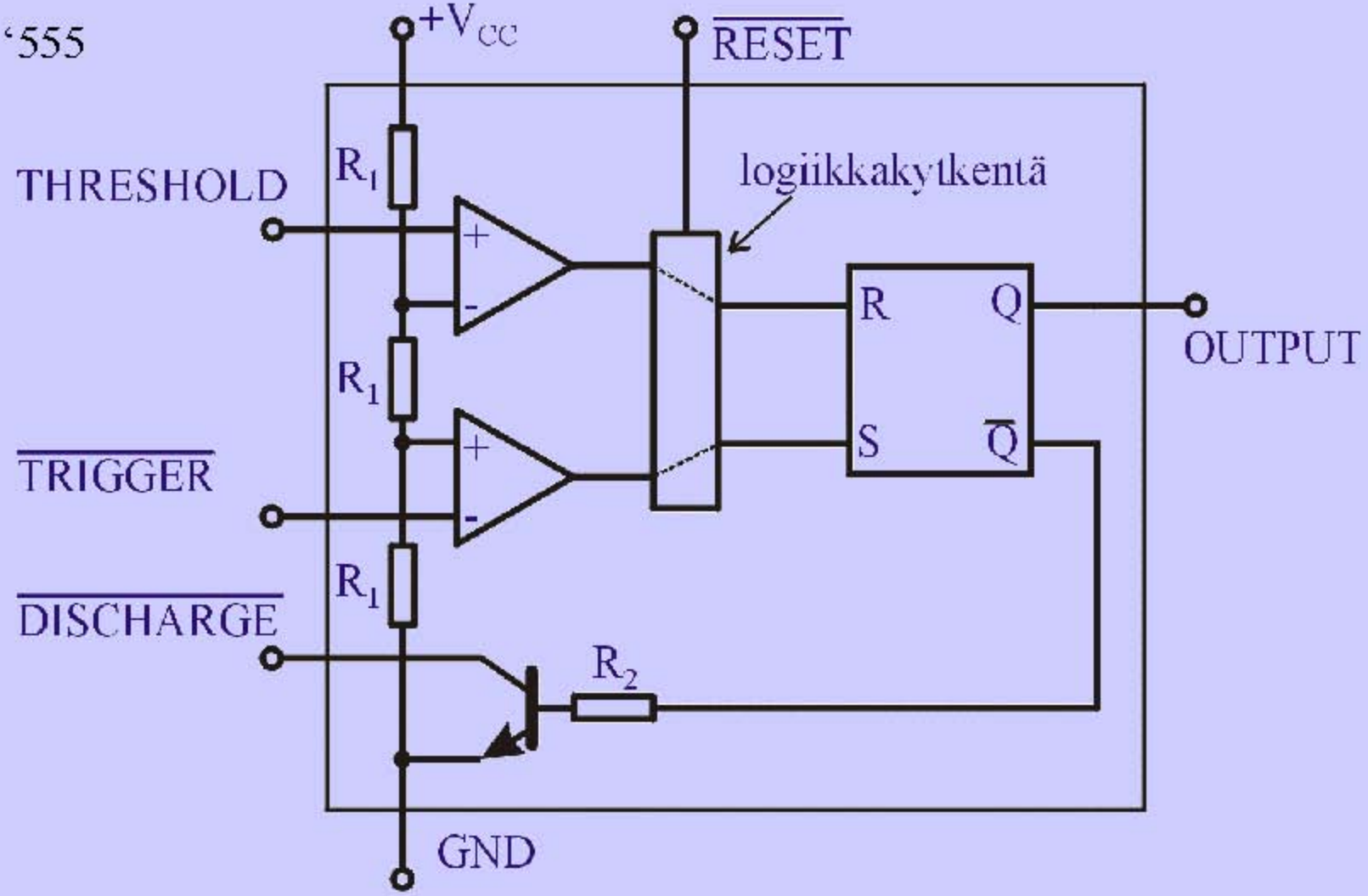


'tasasignaali', jonka jännitearvo vastaa taajuutta

Taajuuden kertojapiiri

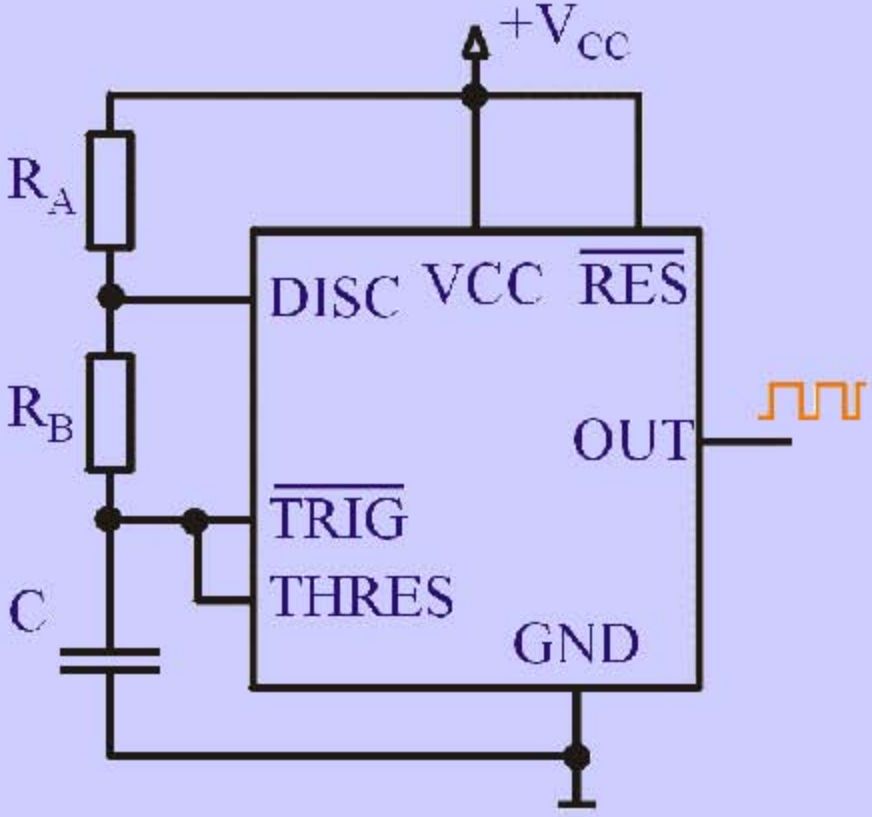


‘555

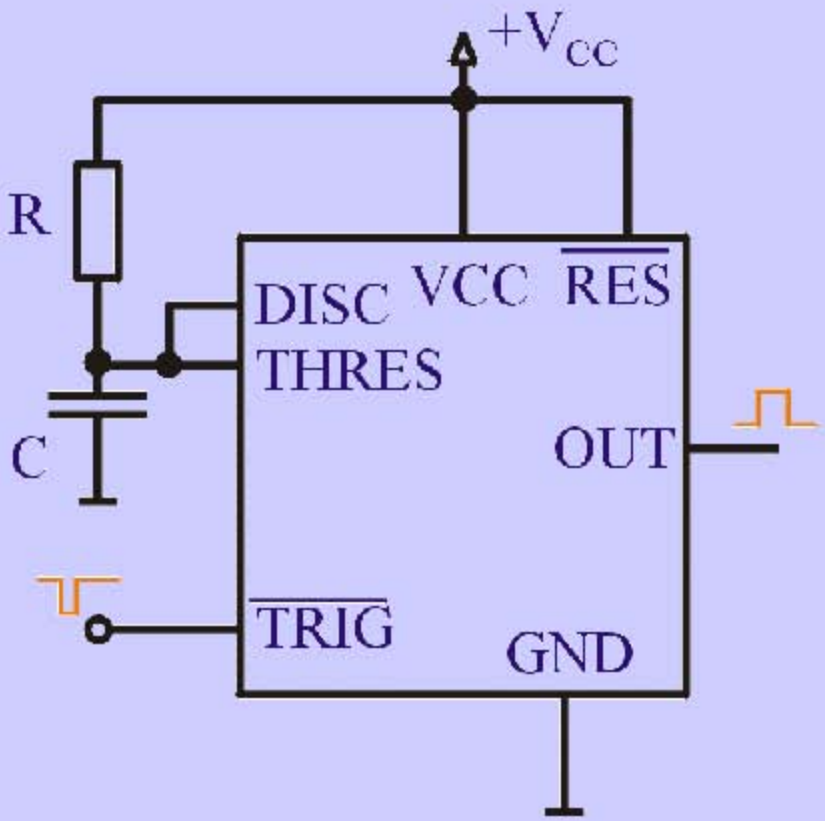

+Vcc
RESET
THRESHOLD
R1
logiikkakytkentä
R
Q
OUTPUT
R1
S
Q
TRIGGER
R1
DISCHARGE
R2
GND

Ajastinkytkentöjä

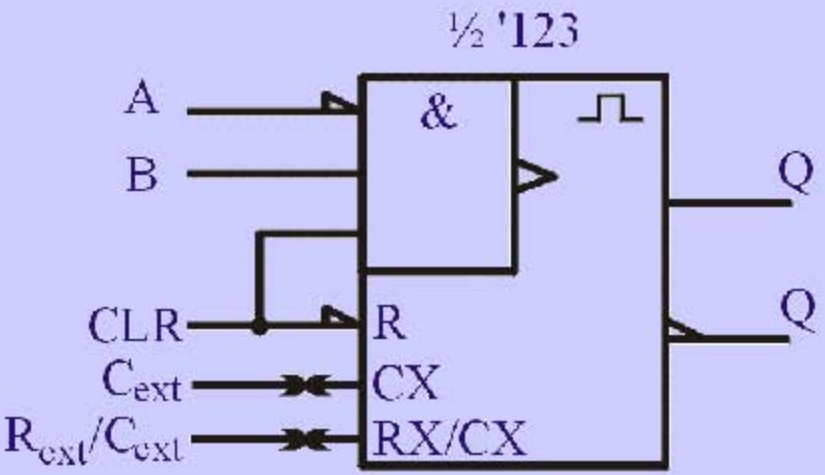
oskillaattori



monostabiili

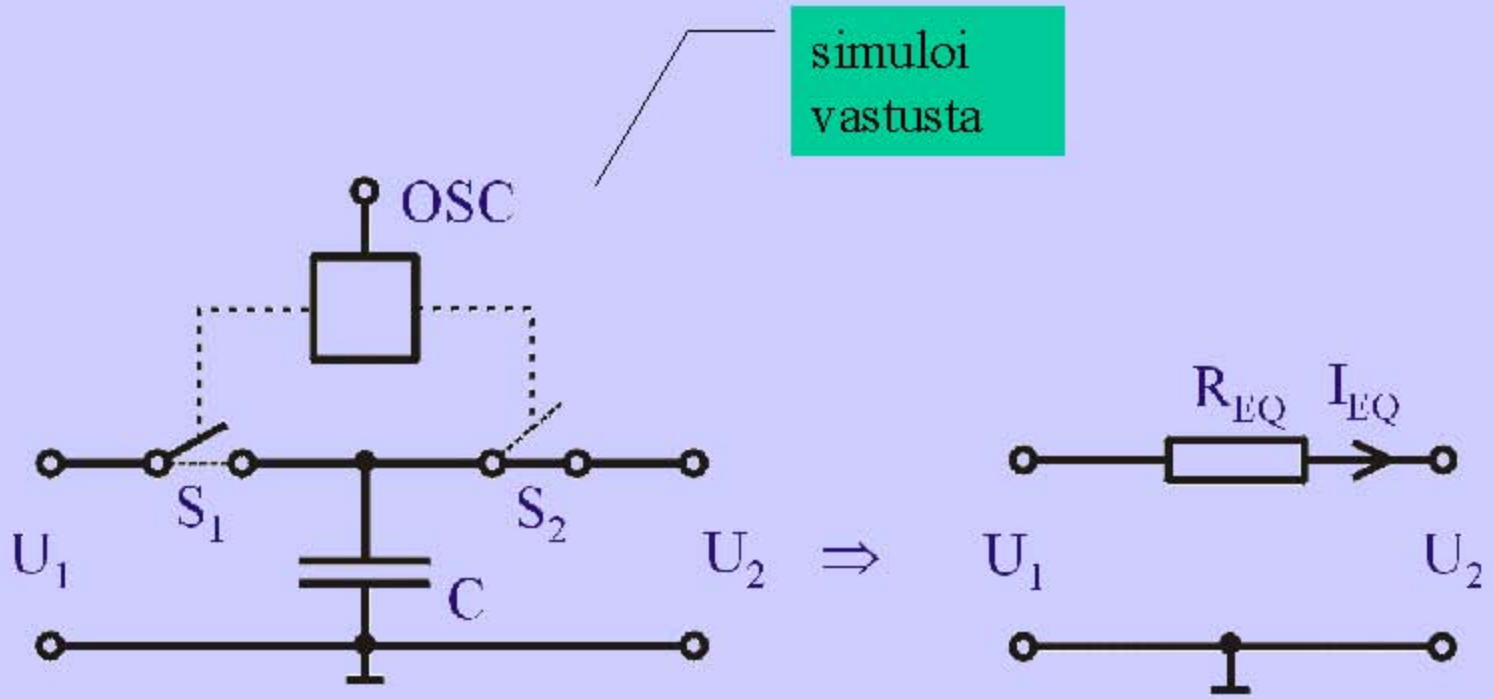


Digitaalilogiikkaperheisiin (esim. HC tai LS) kuuluva monostabiili



INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

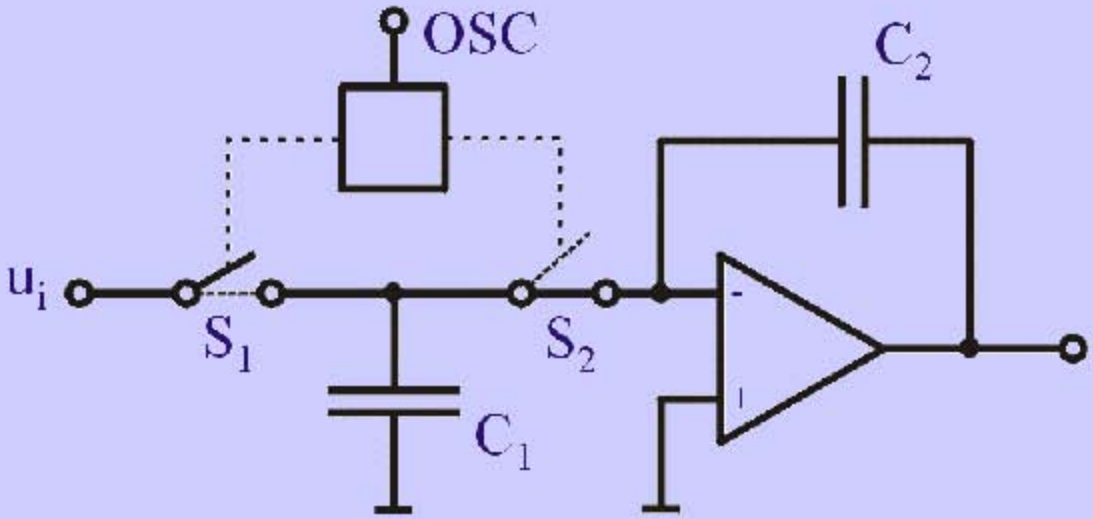
*these lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.



SC = switched capacitor

SC-tekniikalla toteutetut

integraattori



vahvistin